

**WHAT IS CLAIMED IS:**

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1 1. A bonding pad structure disposed on a surface of a  
2 semiconductor substrate with a circuit therein, comprising:  
3 a bottom metal layer disposed over the surface of the  
4 semiconductor substrate to connect the circuit electrically;  
5 an inter-metal dielectric layer disposed over the bottom  
6 metal layer;  
7 a plurality of metal plugs formed therein the inter-metal  
8 dielectric layer to connect with the bottom metal layer;  
9 a top metal layer disposed over the inter-metal  
10 dielectric layer connecting with the metal plugs; and  
11 a passivation layer disposed over the top metal layer  
12 with a plurality of openings to expose the top metal layer  
13 portions as bonding pads, wherein at least one bonding pad is  
14 mark-shaped to indicate the orientation of the bonding pads  
15 on the semiconductor substrate.

1 2. The bonding pad structure as claimed in claim 1,  
2 wherein the mark-shaped bonding pad is a "⊥" shape.

1 3. The bonding pad structure as claimed in claim 1,  
2 wherein the mark-shaped bonding pad is a "⊓" shape.

1 4. The bonding pad structure as claimed in claim 1,  
2 wherein the mark-shaped bonding pad is a cross shape "+".

1 5. The bonding pad structure as claimed in claim 1,  
2 wherein the mark-shaped bonding pad is a "⌈" shape

1 6. The bonding pad structure as claimed in claim 1,  
2 wherein the top and bottom metal layers are an alloy of  
3 aluminum and copper or an alloy of aluminum, copper and  
4 silica.

1 7. The bonding pad structure as claimed in claim 1,  
2 wherein the inter-metal dielectric layer is silicon oxide.

1           8. The bonding pad structure as claimed in claim 1,  
2 wherein the passivation layer is silicon oxide or  
3 borophosphosilicate glass and silicon nitride.

1           9. A probe pad on a semiconductor circuit for electric  
2 characteristic measurement which has a mark-shape to indicate  
3 the relative location of the probe pad on the semiconductor  
4 circuit.

1           10. The probe pad as claimed in claim 9, wherein the  
2 mark-shaped bonding pad is a "□" shape.

1           11. The probe pad as claimed in claim 9, wherein the  
2 mark-shaped bonding pad is a "⌈" shape.

1           12. The probe pad as claimed in claim 9, wherein the  
2 mark-shaped bonding pad is a cross shape "+".

1           13. The probe pad as claimed in claim 9, wherein the  
2 mark-shaped bonding pad is a "⌋" shape.

1           14. The probe pad as claimed in claim 9, wherein the  
2 probe pad is an alloy of aluminum and copper or an alloy of  
3 aluminum, copper and silica.

1           15. A method for forming a bonding pad structure on a  
2 surface of a semiconductor substrate with a circuit therein,  
3 comprising:

4           disposing a bottom metal layer over the surface of the  
5 semiconductor substrate to connect the circuit electrically;

6           disposing an inter-metal dielectric layer over the bottom  
7 metal layer;

8           forming a plurality of metal plugs in the inter-metal  
9 dielectric layer to connect with the bottom metal layer;

10          disposing a top metal layer over the inter-metal  
11 dielectric layer to connect with the metal plugs;

12          disposing a passivation layer over the top metal layer;  
13 and

14          defining a plurality of openings on the passivation layer  
15 to expose the top metal layer portions as bonding pads,

16 wherein at least one bonding pad is defined as a mark-shape  
17 to indicate the orientation of the bonding pads on the  
18 semiconductor substrate.

1 16. The method as claimed as in claim 15, wherein the  
2 mark-shaped bonding pad is defined as a "┐" shape.

1 17. The method as claimed as in claim 15, wherein the  
2 mark-shaped bonding pad is defined as a "┘" shape.

1 18. The method as claimed as in claim 15, wherein the  
2 mark-shaped bonding pad is defined as a cross shape "+".

1 19. The method as claimed as in claim 15, wherein the  
2 mark-shaped bonding pad is defined as a "└" shape.